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| 10/812,958 | 03/31/2004 | Patrice Plante | PAT 2130-2 | 4887 |
| | 7590 04/18/200 ONER GERVAIS LLP | EXAMINER | | |
| Anne Kinsman | | FOUD, HICHAM B | | |
| | HANGE PLAZA FREET SUITE 1100 | ART UNIT | PAPER NUMBER | |
| OTTAWA, ON | | 2619 | | |
| CANADA | | | | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | | Application No. | | Applicant(s) | | | | | |
|--|---|----------------------|----------------|----------------------|--------------------|-------------|--|--|--|
| | | | 10/812,958 | | PLANTE ET AL. | | | | |
| | | | Examiner | | Art Unit | | | | |
| | | | HICHAM B. F | OUD | 2619 | | | | |
| Period fo | The MAILING DATE of this commun or Reply | ication appe | ars on the co | ver sheet with the c | orrespondence ac | idress | | | |
| A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). | | | | | | | | | |
| Status | | | | | | | | | |
| 1) | Responsive to communication(s) file | ed on <i>08 .lan</i> | nuary 2008 | | | | | | |
| ′= | Responsive to communication(s) filed on <u>08 January 2008</u> . This action is FINAL . 2b) This action is non-final. | | | | | | | | |
| 3) | | <i>'</i> — | | | secution as to the | e merits is | | | |
| ٥/١ | Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213. | | | | | | | | |
| | ciocca in accordance with the practi | oo anaor Ex | parto Quay | o, 1000 o.b. 11, 10 | 0.0.210. | | | | |
| Dispositi | on of Claims | | | | | | | | |
| 4)🛛 | Claim(s) <u>1,3-16 and 18-20</u> is/are per | nding in the a | application. | | | | | | |
| | 4a) Of the above claim(s) is/are withdrawn from consideration. | | | | | | | | |
| 5) | 5) Claim(s) is/are allowed. | | | | | | | | |
| 6)🖂 | 6) Claim(s) <u>1, 3-16 AND 18-20</u> is/are rejected. | | | | | | | | |
| · | Claim(s) is/are objected to. | , | | | | | | | |
| • | Claim(s) are subject to restrict | ction and/or e | election real | irement | | | | | |
| ٥,١ | are subject to result | otion and or c | olooiloll loqu | in official. | | | | | |
| Applicati | on Papers | | | | | | | | |
| 9)□ | The specification is objected to by th | e Examiner. | | | | | | | |
| 10) | The drawing(s) filed on is/are: | : a) <u> </u> | oted or b) | objected to by the F | Examiner. | | | | |
| <i>,</i> — | Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a). | | | | | | | | |
| | Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). | | | | | | | | |
| 11) | 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. | | | | | | | | |
| The first caut of declaration is objected to by the Examiner, Note the attached Office Action of John F 10-192. | | | | | | | | | |
| Priority ι | ınder 35 U.S.C. § 119 | | | | | | | | |
| 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. | | | | | | | | | |
| 2) Notic 3) Inform | t(s) e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (F nation Disclosure Statement(s) (PTO/SB/08) r No(s)/Mail Date | PTO-948) | 4) 5) 6) | = | ate | | | | |

Art Unit: 2619

DETAILED ACTION

Response to Amendment

1. The amendment filed on 01-09-2008 has been entered and considered.

Claims 1, 3-16 and 18-20 are pending in this application.

Claims 2 and 17 have been canceled.

Claims 1, 3-16 and 18-20 remain rejected as discussed below.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 3-5, 7-12 and 14-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the added limitation "for storing a single grain for each channel", is vague and unclear because it contradicts with the rest of the limitations which is "selecting data grains prior to storing". Also, in the disclosure, the unselected grains are dropped (see [0028] lines 12-16). Moreover, it is not known what "each channel" refers to.

Claims 3-5, 7-12 and 14-15 are rejected because of their dependency on the rejected claim.

Claim Rejections - 35 USC § 102

Art Unit: 2619

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-4, 7, 8, 10-16 and 18-20 are rejected under 35 U.S.C. 102 (e) as being anticipated by Williams (US 7,113,505).

Claims are rejected as best understood;

For claim 1, Williams discloses a time division multiplexing switch (see Figure 5) comprising: a plurality of ingress ports (see Figure 5 elements 500; 4 input channels), each of the ingress ports in the plurality for synchronously receiving data grains at fixed time intervals (see Figure 5; timeslot #), the data grains ordered as grain groups (see Figure 5; samples order before TSI); at least one memory egress self selection (MESS) egress port (see Figure 5; crossbar and/or Figure 4; outputs), for receiving the data grains from the plurality of ingress ports (see Figure 5; sample order before TSI), for storing a single grain for each channel, and for transmitting stored data grains in a predetermined order (see Figure 5; sample order after TSI), the at least one MESS egress port having a data grain selector for selecting data grains from the received data grains in accordance with at least one predetermined criterion prior to storing the selected grains for transmission by the MESS egress port (see Figure 5 element 502; TSI and/or Figure 1 element 100; TSI), the predetermined criterion being based on the

ingress port associated with the received data grains (see Figure 5; TSI selects data grains from a respective grain group based on each channel which represents associated input port) and a position of a grain in its respective grain group (see Figure 5; TSI reorders the data grains depending on the their positions; see how the order of channel #2 are changed before and after TSI to avoid collision).

Page 4

For claim 3, Williams discloses a time division multiplexing switch, further including a grain aggregator, operatively connected to the plurality of ingress ports, for aggregating the data grains received by each of the ingress ports and for providing the aggregate to the at least one MESS egress port (see Figure 1, MUX).

For claim 4, Williams discloses a time division multiplexing switch, wherein the data grain selector includes an ingress processor for receiving an aggregate of the data grains received by the plurality of ingress ports, and for selecting data grains from the aggregate for storage in accordance with the at least one predetermined criterion (see Figure 1 element 100; TSI).

For claim 7, Williams discloses a time division multiplexing switch, wherein each of the MESS egress ports includes: a memory for storing the selected data grains, the memory including a plurality of RAMs for storing a received grain (see column 9 lines 65-67) and an egress processor for reading and transmitting the stored data grains from the memory in a predetermined order (see Figure 5; sample order after TSI).

For claim 8, Williams discloses a time division multiplexing switch, wherein the ingress processor includes a memory compactor for addressing the selected data

grains for storage in the memory without memory fragmentation (see Figure 5, sample order after TSI; wherein packets are queued without fragmentation).

For claim 10, Williams discloses a time division multiplexing switch, wherein the memory is sized to store exactly one grain group (see Figure 5; time slot #).

For claim 11, Williams discloses a time division multiplexing switch, wherein the memory stores only the selected data grains (see Figure 5; all packets are stored).

For claim 12, Williams discloses a time division multiplexing switch, wherein the egress processor includes an egress processing memory for storing the predetermined order for reading and transmitting the stored data grains (see Figure 5, sample order after TSI).

For claim 13, Williams discloses a time division multiplexing switch comprising: a plurality of ingress ports, each of the ingress ports in the plurality for synchronously receiving data grains at fixed time intervals, the data grains ordered as grain groups (see Figure 1 element 106; MUX); at least one memory egress self selection (MESS) egress port, for receiving the data grains from the plurality of ingress ports and for transmitting stored data grains in a predetermined order (see Figure 5, sample order after TSI), the at least one MESS egress port having a data grain selector for selecting data grains from the received data grains in accordance with at least one predetermined criterion prior to storing the selected grains for transmission by the MESS egress port (see Figure 5, TSI), wherein the data grain selector includes an ingress processor for receiving an aggregate of the data grains received by the plurality of ingress ports, and for selecting data grains from the aggregate for storage in accordance with the at least

one predetermined criterion, wherein each of the MESS egress ports includes (see Figure 5, TSI): a memory for storing the selected data grains (see Figure 5, sample order after TSI), and an egress processor for reading and transmitting the stored data grains from the memory in a predetermined order (see Figure 5; TSI), the egress processor including an egress processing memory for storing the predetermined order for reading and transmitting the stored data grains (see Figure 5, sample order after TSI); and the switch further including a connection memory for storing connection information, for providing an interest RAM with the predetermined criterion and the egress processing memory with the predetermined order in accordance with the stored connection information (see Figure 8 element 810; connection map).

Page 6

For claims 14 and 15, Williams discloses a time division multiplexing switch, wherein the egress processor includes an N:1 or N:M multiplexer attached to the memory for reading and sequentially transmitting the stored data grains in the predetermined order, where N is the number of ingress ports and M>1 (see Figure 1 element 106; MUX).

For claim 16, Williams discloses a method of time division multiplex switching received data grains to at least one egress port, the method comprising: receiving and aggregating a plurality of data grains received in a single timeslot at a number of ingress ports (see Figure 1 element 106; MUX), each of the plurality of data grains being associated with a grain group (see Figure 5 elements 500); transferring the aggregate of the received data grains to the at least one egress port (see Figure 5; sample order before TSI); selecting from the aggregate the data grains to be transmitted by the at

least one egress port (see Figure 5; sample order before and after TSI), including applying a mask to the aggregate to select grains in accordance with the ingress port associated with the position of the grain in the aggregate (see Figure 5; TSI selects data grains from a respective grain group based on each channel which represents associated input port) and the position of the grain in its respective grain group (see Figure 5; TSI reorders the data grains depending on the their positions; see how the order of channel #2 are changed before and after TSI to avoid collision); storing the selected data grains at the least one egress port (see Figure 5; sample order after TSI); and transmitting the stored data grains from the at least one egress port in a predetermined order (see Figure 5; sample order after TSI).

Claim 18 is rejected for same reasons as claim 11.

Claim 19 is rejected for same reasons as claim 8.

For claim 20, Williams discloses a method wherein the step of transmitting includes reading stored grains from the memory in a predetermined order (see Figure 5; sample order after TSI).

Claim Rejections - 35 USC § 103

- 4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams in view of Bianchini (US 7,031,330).

For claim 5, Williams further discloses a time division multiplexing switch, wherein the ingress processor includes an interest memory for storing a grain mask corresponding to the predetermined grain selection criterion (see column 9 lines 65-67) and compacting incoming data grains into data memory at each egress portot remove gaps between the selected grains (see Figure 5; sample order after TSI; wherein there is no gap between timeslots). Williams discloses all the subject matter with the exception of a finite state machine for selecting grains from the aggregate for storage in accordance with the grain mask. However, Bianchini discloses a system that uses Write and Read finite state machine for writing packets into a corresponding queue and from an input queue group into the memory (see column 4 lines 14-24). Thus, it would have been obvious to the one skill in the art at the time of the invention to use a finite state machine as taught by the invention of Bianchini into the invention of Williams for the purpose of writing packets into the memory, since finite state machine is an imaginary machine that is used to study and design systems that recognize and identify patterns.

Claim 6 is rejected for same reasons as claims 1 and 5.

For claim 9, Williams further discloses a time division multiplexing switch having a plurality of multiplexers for multiplexing the selected data grains into the memory (see Figure 1 element 106, MUX). Williams discloses all the subject matter with the exception of a finite state machine for selecting grains for storage. However, Bianchini discloses a system that uses Write and Read finite state machine for writing packets into a corresponding queue and from an input queue group into the memory (see

Art Unit: 2619

column 4 lines 14-24). Thus, it would have been obvious to the one skill in the art at the time of the invention to use a finite state machine as taught by the invention of Bianchini into the invention of Williams for the purpose of writing packets into the memory, since finite state machine is an imaginary machine that is used to study and design systems that recognize and identify patterns.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 3-16 and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

- 6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892.
- 7. Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Art Unit: 2619

When responding to this office action, applicants are advised to clearly point out the patentable novelty which they think the claims present in view of the state of the art disclosed by the references cited or the objections made. Applicants must also show how the amendments avoid such references or objections. See 37C.F.R 1.111(c). In addition, applicants are advised to provide the examiner with the line numbers and pages numbers in the application and/or references cited to assist examiner in locating the appropriate paragraphs.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hicham B. Foud whose telephone number is 571-270-1463. The examiner can normally be reached on Monday - Thursday 10-3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T. Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Art Unit: 2619

/Hicham B Foud/ Examiner, Art Unit 2619 04/12/2008

/CHAU T. NGUYEN/

Supervisory Patent Examiner, Art Unit 2619